REMARKS

Claims 1-3, and 6-28 are pending. By this Amendment claims 4 and 5 are canceled without prejudice or disclaimer; claims 1, and 6-24 are amended; and claims 25-28 are added. Reconsideration in view of the above amendments and following remarks is respectfully requested.

The Examiner is respectfully requested to initial each reference on the PTO-1449 submitted with the November 13, 2003 IDS (post-card receipt attached), sign and date the PTO-1449, and return a copy with the next Office Action per MPEP §609.

Claims 1-24 were rejected under 35 U.S.C. §103(a) over Falster (U.S. Paent 6,849,901). The rejection is respectfully traversed.

The invention of claim 1 provides a silicon wafer having a higher gettering effect, and the invention of claim 6 provides a method for manufacturing the silicon wafer of claim 1. Claim 1 recites that stacking fault nuclei which are formed from agglomeration of interstitial silicon, are distributed throughout the entire in-plane direction, and a density of said stacking fault nuclei is set to a range of between $0.5x10^{8}cm^{-3}$ and $1x10^{11}cm^{-3}$.

In the silicon wafer according to claim 1, instead of BMDs of 50nm to 200nm, stacking fault nuclei of which a maximum diameter is 5μm, and which have a high IG effect, are distributed. Therefore, a high IG effect can be obtained (see page 4, lines 14 to 21).

In contrast, Falster (US6,849,901B2) aims to solve performance problems for SOI substrates caused by agglomerates of crystal lattice vacancies or silicon self-interstitials when silicon wafers are utilized as a source of the device layer (see column 2, lines 2 to 5, 24 to 34, and 46 to 52 of Falster). An object of Falster is to provide a silicon on insulator (SOI) structure having a device layer containing an axially symmetric region of substantial radial width which is substantially free of defects resulting from an agglomeration of crystal lattice vacancies or silicon self-interstitials (see column 2, lines 56 to 61 of Falster).

Therefore, the invention of claim 1, in which stacking fault nuclei formed from agglomeration of interstitial silicon are distributed, and thereby a high IG effect is obtained, is different from Falster, who aims to provide a SOI structure which is substantially free of defects resulting from an agglomeration of crystal lattice vacancies or silicon self-interstitials.

Furthermore, the silicon wafer of claim 1 includes SF nuclei regions in which SF nuclei are distributed throughout the entire in-plane direction of the silicon wafer (see page 13, lines 12 to 16, and FIG. 4B).

In contrast, the SOI structure of Falster includes: a superficial oxide layer having a thickness of 20 to 30Å; a DZ layer located in a range of 10 to 100 μm down from the superficial oxide layer; and a region containing a substantially uniform density of oxygen precipitates located in a medial of the structure (corresponding to the SF nuclei regions of the present invention). The region containing oxygen precipitates of Falster does not substantially include agglomerated intrinsic point defects. Falster defines "agglomerated intrinsic point defects" to mean defects caused by a reaction in which self-interstitials agglomerate to produce dislocation loops and networks, and other such self-interstitial related defects (see the description from column 22, line 66 to column 23, line 24 of Falster). Therefore, the "agglomerated intrinsic point defects" defined by Falster includes the stacking fault nuclei. Accordingly, the SF nuclei regions of the present invention are different from the region containing a substantially uniform density of oxygen precipitates of Falster. As described above, the silicon wafer of claim 1 is not obvious in view of Falster because the object of Falster's invention is clearly different..

Since claims 2 and 3 are dependent on claim 1, claims 2 and 3 are also not obvious in view of Falster.

The method for manufacturing a silicon wafer of claim 6 includes vacancy heat treating and SF nuclei heat treating. In the SF nuclei heat treating, a rate of temperature increase is set to 10°C/minute or less, a heat treatment temperature is set to 1100°C or higher, and said heat treatment temperature is maintained for one hour or more.

In contrast, in Falster, a method for manufacturing a wafer is disclosed in which step S1 of growing a superficial oxide layer, step S2 of annealing rapidly, step S3 of cooling rapidly, and step S4 of an oxygen precipitation heat-treatment are included (see from column 8, line 3, to column 10, line 30 of Falster). Steps S2 and S3 may correspond to the vacancy heat treating of claim 6, and step S4 may correspond to a step of forming a defect-free layer on a surface of the wafer as recited in claim 9.

However, in Falster, an embodiment is provided in which an oxygen annealing step is conducted after step S3 of cooling rapidly (see the third embodiment, especially in column 12, lines 30 to 44). In Example 5 of Falster, step S2 of annealing rapidly (at about 1180°C for about 3 minute in an ammonia-containing atmosphere), step S3 of cooling rapidly, and step S4 of the oxygen precipitation heat-treatment are conducted. Among step S3 and step S4, the oxygen annealing step is conducted under conditions in which the wafer is annealed at

about 1180°C for about 3 minutes in an oxygen-containing atmosphere having an oxygen concentration of about 100%.

The difference between the SF nuclei heat treating of claim 6 and the oxygen annealing step of Falster is annealing time. In claim 6, the temperature of SF nuclei heat treating is maintained for a period of one hour or more. If the temperature is maintained for less than one hour, insufficient interstitial silicon is released when oxygen is precipitated using supersaturated vacancies, and it cannot be agglomerated to form SF nuclei (see page 13, lines 20 to 23 of the present invention). In contrast, the annealing time in the oxygen annealing step of Falster is 3 minutes.

As described above, Falster aims to provide the SOI structure having an device layer containing an axially symmetric region of substantial radial width which is substantially free of defects resulting from an agglomeration of crystal lattice vacancies or silicon self-interstitials. Therefore, the annealing time in Falster must be less than 1 hour to prevent the agglomeration of crystal lattice vacancies or silicon self-interstitials. Accordingly, the method for manufacturing a silicon wafer of claim 6 is not obvious in view of Falster.

Since claims 9 to 28 are dependent directly or indirectly on any one of claims 1 to 8, claims 9 to 28 are also not obvious in view of Falster.

Reconsideration and withdrawal of the rejection of claims 1-24 over Falster are respectfully requested.

In view of the above amendments and remarks, Applicants respectfully submit that all the claims are allowable and that the entire application is in condition for allowance.

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Attorney Docket: 061063-0306825

Should the Examiner believe that anything further is desirable to place the application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,
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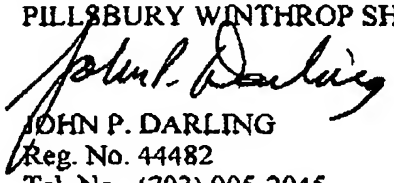

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